REMARKS

This responds to the Office Action mailed on March 14, 2005. No claims are amended, canceled or added. Thus, claims 1-100 remain pending in this application. Of these pending claims, claims 80-100 currently stand withdrawn, and claims 1-79 are being examined. Applicant notes that the Office Action Summary incorrectly lists "claims 10 and 80" as being withdrawn from consideration.

§103 Rejection of the Claims

Claims 54-71 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Han (U.S. 6,611,452) in view of Ashley et al. (U.S. 5,382,814). The rejection recognizes that Han does not disclose the intrinsic region, and asserts that Ashley et al. disclose a semiconductor device with low thermally generated leakage current in column 6 and 7, and further asserts that it would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the required intrinsic region configuration in Han as taught by Ashley et al. in order to have a memory cell with higher performance. Applicant respectfully traverses the rejection, and asserts that the office action does not include a prima facie §103 rejection.

Applicant is unable to find a showing or a fair suggestion of a diode with an intrinsic region in the combination of Han and Ashley et al. The rejection relies on column 6 and 7 of Ashley et al. This portion of Ashley et al. refers to FIG. 2, which illustrates a p+ / p+ / p- / n+ structure, where p+ refers to a heavily doped narrow bandgap p-type region, p+ refers to a relatively wide bandgap heavily doped p-type region, p- refers to a lightly doped p-type region, and n+ refers to a heavily doped narrow bandgap n-type region (col. 4, lines 11-16). As all of these regions are doped, Applicant respectfully submits that the illustrated diode does not include an intrinsic region.

Ashley et al. does refer to the intrinsic contribution to conduction (col. 6 line 53), which is identified as the contribution arising from excitation of valence electrons, as opposed to the extrinsic contribution arising from excitation of impurity states (col. 6 lines 55-57). According to col. 6 lines 36-43, this is a result from the excluding contact 22 (majority carrier holes flow freely from region 16 to region 14 but only a small number of minority carrier electrons flow in reverse direction from region 14 to region 16) and the extracting contact 24 (electrons diffuse

from region 16 to region 18). Definitions of excluding and extracting are provided at col. 2 lines 3-8). Regardless of the effect that the excluding and extracting contacts have on the minority carrier electrons in region 16, Applicant respectfully submits that region 16 is still a doped region (p- region) as illustrated in FIG. 2 and identified in the specification. Thus, Applicant respectfully asserts that Ashley et al. does not show or fairly suggest a diode with an intrinsic region.

Furthermore, Applicant traverses the recited motivation to combine the reference. Applicant is unable to find a fair suggestion in either reference to combine the a p+ / p+ / p- / n+ structure of Ashley et al. with the p+/n/p/n+ thyristor structure (FIG. 2) of Han. The rejection does not clearly state how and why one would combine these structures to form a Negative Differential Resistance (NDR) diode with an intrinsic region between an anode and cathode.

Thus, with respect to independent claim 54, Applicant is unable to find, in the combination of Han and Ashley et al., either a showing or a fair suggestion of the recited memory cell that includes, among other things, a Negative Differential Resistance (NDR) p/i/n diode connected between a diode reference potential line and the second diffusion region where the p/i/n diode includes a p-type anode, an n-type cathode, and an intrinsic region positioned between the anode and the cathode, as recited in the claim. Claims 55-62 depend on independent claim 54, and are believed to be in condition for allowance with claim 54.

Furthermore, with respect to independent claim 63, Applicant is unable to find, in the combination of Han and Ashley et al., either a showing or a fair suggestion of the recited memory cell that includes, among other things, a Negative Differential Resistance (NDR) n/i/p diode connected between a diode reference potential line and the second diffusion region where the n/i/p diode includes an n-type anode, a p-type cathode, and an intrinsic region positioned between the anode and the cathode, as recited in the claim. Claims 64-71 depend on independent claim 63, and are believed to be in condition for allowance with claim 63.

Applicant respectfully requests withdrawal of the §103 rejection, and reconsideration and allowance of the claims.

Allowable Subject Matter

Claims 1-53 and 72-79 were allowed.

Consideration of Withdrawn Claims 80-100

As provided in Applicant's Response to Restriction Requirement dated March 19, 2004, Applicant asserts that claim 1 is a linking claim, insofar as it is a claim to the product linking a process of making and a use (MPEP §809.03) MPEP §809.03 states: *The most common types of linking claims which, if allowed, act to prevent restriction between inventions that can otherwise be shown to be divisible, are . . . (D) a claim to the product linking a process of making and a use (process of using)*).

Applicant also requests the Examiner to consider 37 CFR §1.141(b):

> *Where claims to all three categories, product, process of making, and process of use, are included in a national application, a three way requirement for restriction can only be made where the process of making is distinct from the product. If the process of making and the product are not distinct, the process of using may be joined with the claims directed to the product and the process of making the product even though a showing of distinctness between the product and process of using the product can be made.*

Should the restriction be maintained, Applicant respectfully requests the Examiner to consider claim 1 directed to a memory cell and withdrawn claim 85 directed to a method of forming a memory cell, and to clarify how the process of making is distinct from the product. Additionally, should the restriction be maintained, Applicant respectfully requests an opportunity to address the Examiner's concerns with an appropriate amendment.

As the linking claim is allowed, Applicant respectfully submits that it is proper to withdraw the restriction under MPEP §809. Thus, Applicant respectfully requests consideration and allowance of withdrawn claims 80-100.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6960 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 14 day of June, 2005.

KACIA LEE
Name

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Signature